WHAT IS CLAIMED IS:

1. A method for manufacturing a parallel multi-layer printed circuit board, comprising the steps of:

(A) forming a predetermined number of circuit layers, including the sub-steps of:

(a) forming via holes through a copper stack plate;

(b) plating surfaces of the copper stack plate and inner walls of the via holes with copper; and

(c) forming circuit patterns on the copper stack plate;

(B) forming a predetermined number of insulating layers, including the sub-steps of:

(a) forming via holes through a flat-type insulating material provided with release films attached to surfaces of the flat-type insulating material;

(b) filling the via holes with a conductive paste; and

(c) removing the release films from the flat-type insulating material;

(C) alternately arranging the circuit layers and the insulating layers at predetermined positions;

(D) pressing the arranged circuit and insulating layers; and

(E) forming circuit patterns on the outermost layers of a board obtained by pressing the circuit layers and the insulating layers.

2. The method as set forth in claim 1,

wherein in the sub-step (c) of the step (A), a circuit pattern is formed on one surface of the copper stack plate so as to form the circuit layer arranged on an outermost layer of the printed circuit board, and circuit patterns are formed on both surfaces of the copper stack plate so as to form the circuit layer arranged on an internal layer of the printed circuit board.

3. The method as set forth in claim 1, wherein the step (A) further includes the sub-step of:

(d) surface-treating the copper stack plate.

4. The method as set forth in claim 1, further comprising the step of:

(F) forming a target hole at the position of a target guide mark, serving as a reference point of drilling, on the circuit layers and the insulating layers.

5. The method as set forth in claim 1, wherein the sub-step (a) of each of the steps (A) and (B) includes the

step of:

(a') forming a guide hole at the same position, serving as a reference point of interlayer matching, on the circuit layers and the insulating layers.

6. The method as set forth in claim 1, further comprising the step of:

(C') buffing a portion of the conductive paste, flowing out from the via holes of the outmost layer, so as to remove the protruding portion of the conductive paste, after the step (C).

7. The method as set forth in claim 1,

wherein the release film has a thickness of 20㎛ to 50㎛.

8. The method as set forth in claim 1,

wherein the conductive paste is a metallic bond-type conductive paste impregnated with a tin (Sn) component.

9. The method as set forth in claim 1,

wherein the conductive paste is a point contact-type conductive paste.

10. The method as set forth in claim 1,

wherein the flat-type insulating material includes a resin material in a c-stage, and resin layers in a b-stage respectively stacked on both surfaces of the resin material.

11. A multi-layer printed circuit board comprising:

a plurality of circuit layers, each of the circuit layers provided with a plurality of via holes filled with a conductive paste; and

a plurality of insulating layers, each of the insulating layers provided with a plurality of via holes filled with a conductive paste,

wherein the filling of the via holes of the circuit layers and the via holes of the insulating layers is performed by a process.

12. The multi-layer printed circuit board as set forth in claim 11,

wherein the conductive paste is a metallic bond-type conductive paste impregnated with a tin (Sn) component.

13. The multi-layer printed circuit board as set forth in claim 11,

wherein the conductive paste is a point contact-type conductive paste.